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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,176	KOHLER ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 10/7/08 have been fully considered but they are not persuasive. The remarks on pages 2-4 substantially submit allegedly that Reiner does not "disclose or suggest programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor." Page 2 of Reiner teaches that an object of the invention is a method for programming an OTP memory device comprising ... a MOS memory transistor. Furthermore, pages 3-4 of Reiner inarguably teach that a programming voltage level above the normal operating voltage level is used, and that as a result of such high voltage levels **hot carrier effects** occur in a transistor. Moreover Reiner teaches that "[i]t has thus to be ensured that **no intolerable** degradation of the memory circuitry occurs due to proposed high programming voltage." And that hot carrier conditions resulting in **degradation**, however, are avoided. That is, while hot carrier effects due to high voltage programming occur, inherently leading to transistor physical/electrical degradation, **intolerable degradation** is avoided; after all, the goal of any invention is to have a working invention, not one that is rendered useless due to **intolerable degradation**. Reiner on page 7 furthermore teaches that "even in case the gate oxide of a programmed memory transistor has broken down, this cell will still allow a leakage current and be considered as programmed." That is, high-voltage induced hot carrier conditions can damage the gate oxide, but the damage is within controlled parameters. This is equivalent to FIG. 4 of the instant application, wherein drain junction oxide

damage is illustrated due to a stress voltage Vd_{stress} applied at the drain junction area. As such, for at least these reasons the previous rejection stands.

Allowable Subject Matter

2. **Claim(s) 6 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: the pertinent prior art of record does not teach or suggest, in combination with intervening claim limitations, the steps of raising a source terminal for each of said array of transistors to a positive potential; raising a gate terminal for all transistors along a selected mw to a positive potential and detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim(s) 1-5, 7-15 and 17-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 2004/053889 A1 to Reiner ("Reiner") in view of U.S. Patent No. 5257225 to Lee ("Lee") and U.S. Publication Characterization of Oxide Trap and

Interface Trap Creation During Hot-Carrier Stressing of n-MOS Transistors Using the Floating-Gate Technique to Doyle et al. ("Doyle").

As to claim 1-2, Reiner teaches a method for programming a one time programmable memory (See Abstract), comprising the steps of obtaining an array of transistors (Page 7, lines 12-13); and programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor (FIG. 1 shows memory transistor T2; Page 5, lines 19-page 6, down to line 19 disclose thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction), wherein the hot carrier aging technique comprises injection of carriers into a gate oxide (Page 7, lines 7-11 disclose gate oxide breakdown as induced by hot carriers resulting from T2 being voltage/current biased as disclosed on pages 5-6).

Reiner does not expressly disclose wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps.

However Rainer does teach at page 7, lines 7-11 oxide breakdown as obviously induced by degradation by hot carrier mechanism: trapping electrons.

Moreover, Lee also teaches in the context of OTP memory devices "filling up the traps in the dielectric region" at Column 4, lines 67-column 5, down to line 2.

And Doyle teaches trap creation during hot-carrier stressing of n-MOS transistors (See abstract, at least).

Reiner and Lee and Doyle are analogous art because they are from the same filed of endeavor regarding semiconductor circuit design, in particular transistors having hot carrier induced effects.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate teachings of injection of carriers causes at least one of, the creation of traps, and the filling of traps by Lee and Doyle in the above claim limitation rejection. The suggestion/motivation would have been obvious to one of ordinary skill in the art to conclude that injection of carriers, as induced by voltage/current biasing of a transistor device can cause oxide degradation resulting in charge trapping.

Therefore, it would have been obvious to combine Reiner with Lee and Doyle to make the above modification.

As to claim 3, Reiner teaches said altered characteristic is a change in a threshold voltage of' said at least one of' said transistors (Page 6, lines 27-31 teach that T2 of FIG. 1, when not programmed in a reading operation, will not conduct current; yet when T2 is programmed, in contrast, it will conduct current, obviously changing the threshold voltage of the memory T2).

As to claim 4, Reiner teaches said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of' said of said at least one of' said transistors (Page 5, lines 7-page 6, down to line 7).

As to claim 5, Reiner teaches the step of detecting said programmed at least one of' said transistor by sensing said change in said threshold voltage of said at least one of said transistors (Page 6, lines 27-page 7, down to line 6 teach detecting current of a programmed memory T2 and a non-programmed memory, the current conduction changing accordingly, and therefore detecting change in the threshold voltage which as well known is directly proportional to the conductive current of the memory transistor T2).

As to claim 7, Reiner teaches that said altered characteristic is a change in a saturation current of said at least one of said transistors (Page 6, lines 27-page 7, down to line 6 teach a change of current of programmed memory transistor T2 in FIG. 1 in comparison to a non-programmed memory transistor).

As to claim 8, Reiner teaches said programming step further comprising the step of applying a stressful voltage to a source and a gate of' said at least one of said transistor to cause said change in said saturation current of said of said at least one of' said transistors (Pages 5-6 teach programming of cell T2 in FIG. 1 hot-carrier stressing the drain terminal; as is well known, a source terminal is identical in functionality to a drain terminal in a MOS transistor, as such programming the source terminal follows the same teachings).

As to claim 9, Reiner teaches the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of' said transistors (Page 6-7 teach detecting in a reading

operation of the change in current of a programmed memory T2 in contrast to a non-programmed memory transistor).

As to claim 10, Reiner teaches said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive potential; raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of' voltage decay of at least one column in said array of transistors (Page 6, line 22-23 teach raising a bit (column) line voltage to Vop while in a reading operation and detecting the current level change (voltage level change since Voltage is directly proportional to Current: V=(load)*I, where I is current, as well known)).

As to claim 11-12, see rejection to claims 1-2; furthermore a circuit (readout means) for sensing altered characteristics of said at least one of said transistors is taught on page 6, line 20-21.

As to claim 13, see rejection to claim 3.

As to claim 14, see rejection to claim 4.

As to claim 15, see rejection to claim 5.

As to claim 17, see rejection to claim 7.

As to claim 18, see rejection to claim 8.

As to claim 19, see rejection to claim 9.

As to claim 20, see rejection to claim 10.

As to claim 21, see rejection to claim 1-2; furthermore the teachings of Reiner are in the context of an OTP (See at least page 1, lines 6-8).

As to claim 22, see rejection to claim 7.

As to claim 23, see rejection to claim 3.

As to claim 24, Reiner teaches a memory cell, comprising only one transistor, wherein said transistor comprises: a source region; a drain region; a channel region; one silicon-dioxide gate insulator layer; and one gate electrode layer (Page 5, line 9 teaches of a memory cell: transistor T2 of FIG. 1, which, as illustrated and well known in the art comprises a source region, a drain region, a silicon dioxide above the channel region and below the gate electrode).

As to claim 25, see rejection to claim 1-2.

As to claim 26, Reiner teaches a plurality of said memory cells arranged in an array of rows and columns (Column 7, lines 12-13 teach an array of memory cells T2 of FIG. 1; an array of a memory is an arrangement of rows and columns of memory cells as well known; further, Merriam-Webster Dictionary defines array as elements arranged in rows and columns).

As to claim(s) 27-28, see rejection to claim 11-12.

As to claim 29, see rejection to claim 13.

As to claim 30, see rejection to claim 15.

As to claim 31, see rejection to claim 7.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando N. Hidalgo/
Examiner, Art Unit 2827

/Huan Hoang/
Primary Examiner, Art Unit 2827